WHAT IS CLAIMED IS:

1. A semiconductor memory chip comprising:

a plurality of wells of a first conduction type, each well formed in a substrate and containing a first set of active components and a first set of contacts associated with the first set of active components; and

a plurality of wells of a second conduction type, each well formed in a substrate and containing a second set of active components and a second set of contacts associated with the active components,

wherein the wells of the first conduction type share a mutually adjoining boundary with the wells of the second conduction type,

wherein the first set of contacts and second set of contacts lie in region near the mutually adjoining boundary, and

wherein the active components lie further away from the mutually adjoining boundary than do the first and second set of contacts.

2. The memory chip of claim 1, wherein the memory chip comprises a DRAM chip.

3. The memory chip of claim 1, wherein the circuit layout structures are not mirror-symmetrical with respect to a center line therein.

4. The memory chip of claim 2, wherein the circuit layout structures are not mirror-symmetrical with respect to a center line therein.

5. The memory chip of claim 3, wherein the wells of the first conduction type are p-type, and include n-channel FETs fabricated thereon, and

wherein the wells of the second conduction type are n-type, and include p-channel FETs fabricated thereon.

6. The memory chip of claim 4, wherein the wells of the first conduction type are p-type and include n-channel FETs fabricated thereon, and

wherein the wells of the second conduction type are n-type, and include p-channel FETs fabricated thereon.

7. A method for fabricating an integrated semiconductor memory chip, comprising:

implanting using an ion beam at oblique incidence a plurality of wells of a first conduction type;

implanting using an ion beam at oblique incidence a plurality of wells of a second conduction type, wherein the wells of the first conduction type share a mutually adjoining boundary with the wells of the second conduction type;

forming a first set of active components on the wells of the first conduction type;

forming a second set of active components on the wells of the second conduction type;

forming a first set of contacts to the wells of the first conduction type; and

forming a second set of contacts to the wells of the second conduction type,

wherein the first set and second set of contacts lie in a region near the mutually adjoining boundary, and

wherein the first and second set of active components lie further away from the mutually adjoining boundary than do the first and second set of contacts.

8. The method of claim 7, wherein the arrangement of circuit layout structures is not mirror-symmetrical with respect to a center line within the memory chip.

9. The method of claim 8, wherein the wells of the first conduction type are p-type, and include n-channel FETs fabricated thereon, and

wherein the wells of the second conduction type are n-type, and include p-channel FETs fabricated thereon.

10. A DRAM memory chip architecture comprising:

a plurality of pairs of wells, each pair including an n-type well adjacent to a p-type well,

wherein a border region is defined along an edge where each n-well and p-well are mutually adjacent;

a set of contacts within each well arranged to lie within the border region; and

a set of active components within each well arranged to lie outside the border region.

11. The DRAM chip architecture of claim 10, wherein the arrangement of the pairs of wells is such that there is no mirror symmetry of the well location with respect to a line through the center of the chip.

12. The DRAM chip architecture of claim 11, wherein a contamination zone due to implantation scattering during well implantation lies within the border region within each pair of wells.